CLAIMS

What is claimed is:

1. A method for testing AC coupled interconnects of a circuit having a transmitting IC and a receiving IC that are coupled together by an AC interconnection, each IC having a Boundary Scan Cell (BSC) connected to a reference clock and a source of an input signal, the method comprising:

generating an AC signal based on a value of the BSC of the transmitting IC and the reference clock;

transmitting a sync pulse signal to the BSC of the receiving IC;

capturing a phase of said AC signal in relation to said sync pulse signal;

capturing a phase of the input signal;

comparing the phase of the input signal with the phase of said AC signal in relation to said sync pulse signal; and

sending an output signal based on said comparing.

2. The method according to claim 1, wherein said generating further comprises resetting the BSC of the transmitting IC.

3. The method according to claim 2, wherein said resetting further comprises generating a zero value signal in a boundary scan register.

4. The method according to claim 1, wherein said sync pulse further captures a default phase.

5. The method according to claim 1, wherein said output signal further comprises the inverted phase of said sync pulse signal when the phase of the input signal does not match the phase of said AC signal in relation to said sync pulse signal.

6. The method according to claim 1, wherein said output signal toggles whenever the phase of the input signal changes.

7. The method according to claim 1, wherein said capturing a phase of said AC signal in relation to said sync pulse signal further comprises storing the phase of said AC signal in relation to said sync pulse signal.

8. A system for testing AC coupled interconnects of a circuit having a driving IC and a receiving IC that are coupled together by an AC interconnection, each IC having a plurality of boundary scan cells (BSCs), the system comprising:

means for generating an AC signal based on a value of the BSC of the transmitting IC and the reference clock;

means for transmitting a sync pulse signal to the BSC of the receiving IC;

means for capturing a phase of said AC signal in relation to said sync pulse signal;

means for capturing a phase of the input signal;

means for comparing the phase of the input signal with the phase of said AC signal in relation to said sync pulse signal; and

means for sending an output signal based on said comparing.

9. The method according to claim 8, wherein said means for generating further comprises means for resetting the BSC of the transmitting IC.

10. The method according to claim 9, wherein said means for resetting further comprises generating a zero value signal in a boundary scan register.

11. The method according to claim 8, wherein said sync pulse further captures a default phase.

12. The method according to claim 8, wherein said output signal further comprises the inverted phase of said sync pulse signal when the phase of the input signal does not match the phase of said AC signal in relation to said sync pulse signal.

13. The method according to claim 8, wherein said output signal toggles whenever the phase of the input signal changes.

14. The method according to claim 8, wherein said capturing a phase of said AC signal in relation to said sync pulse signal further comprises means for storing the phase of said AC signal in relation to said sync pulse signal.

15. A program storage device readable by a machine, tangibly embodying a program of instructions readable by the machine to perform a method for testing an AC coupled interconnect of a circuit having a transmitting IC and a receiving IC that are coupled together by an AC interconnection, each IC having one BSC connected to a reference clock and an input signal, the method comprising:

generating an AC signal based on a value of the BSC of the transmitting IC and the reference clock;

transmitting a sync pulse signal to the BSC of the receiving IC;

capturing a phase of said AC signal in relation to said sync pulse signal;

capturing a phase of the input signal;

comparing the phase of the input signal with the phase of said AC signal in relation to said sync pulse signal; and

sending an output signal based on said comparing.

16. The method according to claim 15, wherein said generating further comprises resetting the BSC of the transmitting IC.

17. The method according to claim 16, wherein said resetting further comprises generating a zero value signal in a boundary scan register.

18. The method according to claim 15, wherein said sync pulse further captures a default phase.

19. The method according to claim 15, wherein said output signal further comprises the inverted phase of said sync pulse signal when the phase of the input signal does not match the phase of said AC signal in relation to said sync pulse signal.

20. The method according to claim 15, wherein said output signal toggles whenever the phase of the input signal changes.

21. The method according to claim 15, wherein said capturing a phase of said AC signal in relation to said sync pulse signal further comprises storing the phase of said AC signal in relation to said sync pulse signal.

22. An output AC boundary scan cell comprising:

a first flip-flop having a data input connected to a *bscanShiftIn* line, a clock input connected to a *clockBscanAc* line, a test reset input connected to a *testBscanAc* line, an output connected to a *bscanShiftOut* line;

a second flip-flop having a data input connected to said output of said first flip-flop, an update input connected to a *updateBscanAc* line, and a second flip-flop output;

an XOR logic gate having a first input connected to a *refClk* line, and a second input connected to said second flip-flop output, and an XOR logic gate output; and

a multiplexor having a first input connected to a *fromCore* line and a *selectJtagOut* line, and a second input connected to said XOR logic gate output, and a multiplexor output.

23. An output AC boundary scan cell generating a signal, said output AC boundary scan cell comprising:

a first flip-flop for resetting the output AC boundary scan cell;

a second flip-flop connected to said first flip-flop for updating the output AC boundary scan cell;

an XOR logic gate connected to said second flip-flop for generating the signal; and

a multiplexor for sending the signal.

24. An input AC boundary scan cell comprising:

a first flip-flop having a data input, a clock input connected to a *refClk* line, a first flip-flop output;

a first multiplexer having a first input connected to a syncPulse line, a second input connected to said first flip-flop output, a first multiplexer output;

a second flip-flop having a data input connected to said first multiplexer output, a clock input connected to a *refClk* line, and a second flip-flop output feedback to said first input of said first multiplexer;

an XOR logic gate having a first input connected to said second flip-flop output, a second input connected to said first flip-flop output, and an XOR logic gate output;

a second multiplexer having a first input connected to said first flip-flop output and an *acjtagMode* line, a second input connected to said XOR logic gate output, and a second multiplexer output;

a third multiplexer having a first input connected to a *bscanShiftIn* line and a *ShiftBscan2Edge* line, a second input connected to said second multiplexer output, a third multiplexer output; and

a third flip-flop having a first input connected to said third multiplexer output, a second input connected to a *clockBscan* line, and a third flip-flop output connected to a *bscanShiftOut* line.

25. An input AC coupled boundary scan cell for receiving a signal comprising:

a sampling flip-flop for sampling an input signal with respect to a reference clock;

a feedback flip-flop connected to said sampling flip-flop for controlling the signal; and

a multiplexer connected to said sampling flip-flop and said feedback flip-flop for decoding the signal.

26. The input AC coupled boundary scan cell according to claim 25 further comprising a shifting out flip-flop connected to said multiplexer for processing the signal.